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APPLICANTS

Peter H. Alfke, Los Altos Hills, CA;  
 Himanshu J. Verma, Mountain View, CA;

\*\* CONTINUING DATA *YES H/R* \*\*\*\*\*  
 This application is a DIV of 10/198,801 07/19/2002 PAT 6,734,703

\*\* FOREIGN APPLICATIONS *NONE H/R* \*\*\*\*\*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED  
 \*\* 05/31/2004

Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after Allowance <i>Ellen Koshalek HE</i> Examiner's Signature Initials	STATE OR COUNTRY CA	SHEETS DRAWING 6	TOTAL CLAIMS 18	INDEPENDENT CLAIMS 3
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ADDRESS  
 24309  
 XILINX, INC  
 ATTN: LEGAL DEPARTMENT  
 2100 LOGIC DR  
 SAN JOSE , CA  
 95124

TITLE  
 Circuits and methods for analyzing timing characteristics of sequential logic elements

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